EN11348

Frequency Threshold Audio Activity Detector

BACKGROUND

TECHNICAL FIELD

5 This invention relates generally to audio detection circuits, and more particularly to

filtering detection circuits employing digital counters to actuate a loudspeaker.

BACKGROUND ART

Modern digital cellular telephones communicate using predominantly three protocols:

10 Time Division Multiple Access (TDMA); Code Division Multiple Access (CDMA) and the

Global System for Mobile communications (GSM). Each different protocol transmits digital data

in a different manner. TDMA divides the call into three time slots, so as to transmit more data.

CDMA causes the digital signal to vary according to a defined pattern or "code" before it is

transmitted in a spread spectrum. GSM, which is the most popular protocol in the world, digitizes

15 and compresses the digital signal, and then sends it down a channel with other streams of data,

each in its own time slot.

In each of these three protocols, data is transmitted in packets or "bursts". The bursts can

be problematic for audio engineers because the amplifiers in the phone require large pulses of

current to transmit them. These large bursts of current can create noise in the circuitry of the

20 phone. If not properly contained, the noise can be heard on the earpiece loudspeaker. Such noise

can degrade the quality of cellular calls.

For example, referring now to FIG. 3, illustrated therein is a typical GSM current

waveform 300. The waveform 300 illustrates the current drawn by the phone's power amplifiers

from the battery or power supply. The waveform 300 includes a nominal component 301 that is

25 generally on the order of 250 mA. The waveform includes a pulse 302 having a peak 303

amplitude of about 1.7 A and an average of about 1.4 A. The pulse frequency 305 is 217 Hz and the duty cycle 306 is 12.5%. As the frequency 305 is within the audible range of humans, if this waveform couples into the phone's loudspeaker it can become quite a nuisance.

The problem is compounded in speakerphone applications. As power is drawn through

5   the same connector as the audio signal, the pulse waveform often couples to the audio lines. When the cellular phone is coupled to a speakerphone accessory, and the phone is not in a call, the speakerphone must be muted less the user hear an annoying 217 Hz buzz. However, when a call is in place, the speaker must be actuated. Thus, the speakerphone must be able to determine the difference between the 217 Hz pulse and actual audio in order to be able to mute the speaker

10   when no audio is present.

One possible solution to this problem would be to couple the audio signal through a high pass filter that filters out all frequencies above about 220 Hz. Such filters include high order (fourth order or more) Butterworth and Chebychev filters comprising resistors, capacitors and inductors. The problems with these filters are threefold: First, high-order filters require numerous

15   components and can thus be quite expensive. Second, high order filters introduce poles and zeroes into the frequency response that may cause stability problems in the overall circuit. Third, since the 217 Hz is within the audio range, filtering frequencies below this amount will truncate a portion of the audio information.

There is thus a need for an improved audio detection and filtering circuit.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a preferred embodiment of an audio detection and filtering circuit in accordance with the invention.

FIGS. 2(a)-2(e) illustrates exemplary waveforms associated with different nodes of an audio

25   detection and filtering circuit in accordance with the invention.

FIG. 3 is an exemplary GSM current waveform associated with portable communications devices.

DETAILED DESCRIPTION OF THE INVENTION

5   A preferred embodiment of the invention is now described in detail. Referring to the drawings, like numbers indicate like parts throughout the views. As used in the description herein and throughout the claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise: the meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on."

10   Referring now to FIG. 1, illustrated therein is a preferred embodiment of an audio detection and filtering circuit 100 in accordance with the invention. As noted above, one goal of the invention is to mute a loudspeaker when no call is in progress, where 217 Hz pulses may parasitically appear on the audio lines, and actuate the loudspeaker when audio signals are present. The invention thus solves this problem by inactivating the loudspeaker when frequencies

15   below a predetermined threshold are present, and by actuating the loudspeaker when frequencies above a predetermined threshold are present. This is best explained by way of example.

Audio signals are coupled to the circuit 100 at the input node 101. In this particular embodiment, an optional capacitor 102 provides AC coupling to an amplifier, however the circuit 100 operates equally well with DC coupling. DC coupling is appropriate where the audio signal

20   has a sufficient DC bias as to operate in the circuit's preferred operational range. From this point, the audio signal is amplified via a traditional amplification circuit like the op-amp 103 illustrated here.

From the initial amplification, the audio signal is coupled to a secondary amplifier 113 and simultaneously to a resistor divider comprised of resistors 104 and 105. Resistor 104 is

typically much smaller in value than resistor 105. These resistors 104,105 provide a means of scaling the amplified audio signal.

From the resistor divider 104,105, the audio signal is coupled to a comparator 108. The comparator 108 compares the amplified audio signal to a reference 106. The comparator 108 thus

5   outputs a pulse train that corresponds to the frequency of the audio signal. When only the 217 Hz waveform is present, the output of the comparator is, of course, a 217 Hz pulse train. However, when audio is present, the audio has frequencies in excess of 217 Hz, and thus the pulse train becomes much higher in frequency. Optional resistor 107 provides hysteresis where necessary.

The pulse train is coupled to an edge triggered flip-flop array, shown in this case as a

10   ripple counter comprising counter 109 and counter 110. In this preferred embodiment the ripple counter is a two-stage counter. It will be clear to those having ordinary skill in the art, however, that any number of counters may be used depending upon the application.

Counter 109 and 110 are driven by a clock 115 signal that is coupled to the reset pins 116. The clock 115 establishes a "window" during which pulses applied to the input of the ripple

15   counter are clocked completely through counter 109 and counter 110. By tailoring the clock's 115 frequency and duty cycle, one may design a frequency threshold below which no input pulses will pass through the counters 109,110.

By way of example, in the problem stated above it is desirable to mute the speaker 114 below about 250 Hz and enable the speaker 114 for frequencies higher than 250 Hz. If the clock

20   115 frequency is set to 120Hz with a duty cycle of 50%, the "window" created is expressed as

$$1/(120 * 2) = 4.1 \text{ ms} \qquad\qquad \text{(Eq. 1)}$$

Beyond the 4.1 msec window, counter 109 and counter 110 are reset. For the output 117 of counter 110 to change, the pulse train from the comparator must have a frequency greater than 240 Hz, which corresponds to at least two pulses within the 4.1 ms window.

Once the output 117 of counter 110 changes, this actuates the secondary amplifier 113. Once the output 117 of counter 110 changes, the blocking diode 111 and resistor-capacitor combination 112 ensure that the output from the ripple counter remains active for at least one clock 115 reset cycle. This delay prevents the secondary amplifier 113 from going inactive at

5   each ripple counter reset. Thus, a period of a least two clock cycles without pulses greater than 240 Hz must pass for the secondary amplifier 113 to be disabled.

It is well to note that the flip-flops 109,110 of FIG.1 have been drawn in a generic notation. It is known in the art that counters may be constructed with various types of flip-flops including D-latch flip flops, J-K flip-flops and S-R flip-flops. The specific configuration of each

10   counter depends upon the type of flip-flop. For example, using a J-K flip-flop requires the J-K inputs of the first flip-flop to be tied high, while a D-latch flip-flop requires the D-input to be tied to the Q-bar output. On-Semiconductor offers many informative application notes for flip-flops, including the MC14027B dual J-K flip-flop. While the circuits are known to those having ordinary skill in the art, the application notes offer helpful explanations and schematics of

15   application circuits.

Referring now to FIG. 2, illustrated therein are waveforms corresponding to the circuit of FIG. 1. FIG. 2(a) illustrates a series of GSM pulses 205 with a frequency of about 217 Hz. These pulses 205 represent the noise presented to an audio accessory by the phone.

FIG. 2(b) illustrates an exemplary audio output. This output corresponds to the signal

20   present at node 101 of FIG. 1. In region 201, where no audio signal is present, the voltage is essentially zero. In region 202, an audio signal 204 is present. As the human ear perceives frequencies between 20 Hz and 20kHz, the audio signal 204 will include frequency components in excess of 240 Hz.

FIG. 2(c) illustrates the output of a comparator (element 108 of FIG. 1) when the sum of

25   the GSM pulses 205 of FIG. 2(a) and the audio signal 204 of FIG. 2(b) are compared to a voltage

threshold 206. The result is a pulse-train 207 corresponding to the input signals 204,205. This pulse train corresponds to the signal delivered to the flip-flops 109,110 of FIG. 1.

FIG. 2(d) illustrates the clock signal 208 that is coupled to the counters. The clock signal 208 corresponds to the signal applied to the flip-flops 109,110 at node 116 in FIG. 1. The

5   exemplary clock signal 208 shown here is 120 Hz with a 50% duty cycle.

FIG. 2(e) illustrates the enable signal 209 coupled to the secondary amplifier 113 of FIG. 1. Recall that two pulses must pass within one window to actuate the enable signal 209. This occurs at point 201. The enable signal would normally go to zero while the clock 208 is low, however the resistor-capacitor 112 of FIG. 1 cause a decay as illustrated by curve 211. The

10   enable signal 209 finally drops below the "on" threshold at point 213.

Refer now back to FIG. 1. In the manner described above, the loudspeaker 114 is disabled when frequencies below 240 Hz are present at the audio input 101, but is actuated when frequencies above this threshold are present. Additionally, the circuit 100 is amplitude independent, which means that the amplitude of the input is irrelevant. As long as the amplitude

15   is sufficient to pass the voltage reference 106 present at the comparator 108, the signal will sufficiently enable the secondary amplifier 113. The result is a quiet loudspeaker below a threshold frequency and an active loudspeaker above this frequency. The invention thus provides improved audio quality.

While the preferred embodiments of the invention have been illustrated and described, it

20   is clear that the invention is not so limited. Numerous modifications, changes, variations, substitutions, and equivalents will occur to those skilled in the art without departing from the spirit and scope of the present invention as defined by the following claims. For example, while the predetermined threshold of this example was set to 240 Hz, it will be clear that this threshold is easily changed by altering the number of counters, the clock frequency and the clock duty

25   cycle.